SEMICONDUCTOR MANUFACTURING FOOTPRINT: SUSTAINABILITY AS ROADMAP METRIC

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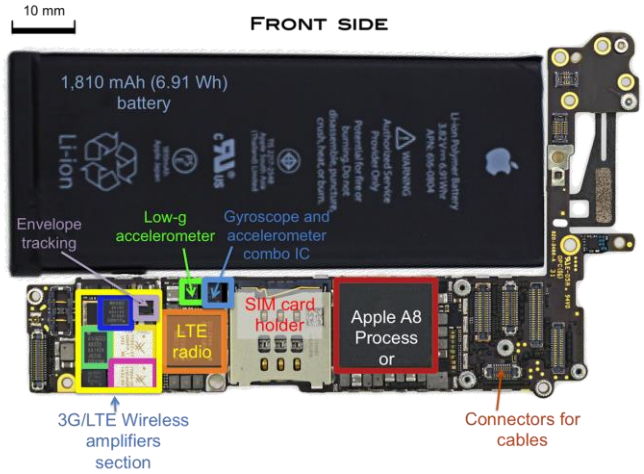
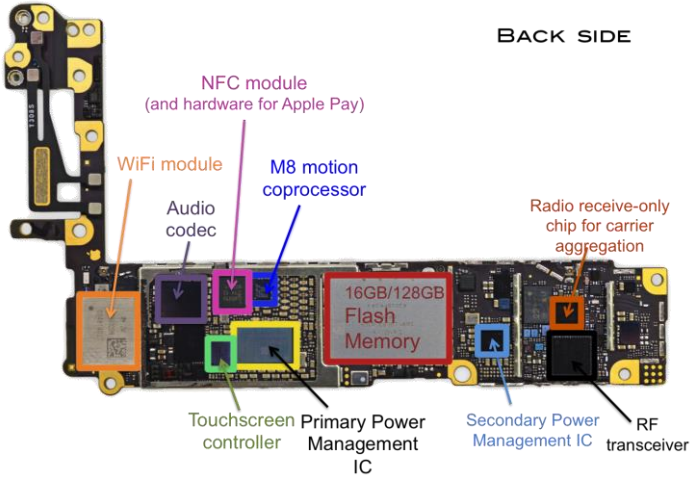
SEMICONDUCTOR TECHNOLOGIES IN ELECTRONICS SYSTEMS
EXAMPLE OF A SMARTPHONE

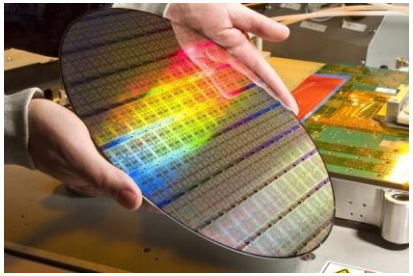
- Battery, display, magnets, PCB
  - Contains REE, gold, Silver.., bulk material
- Semiconductor technologies= integrated circuits : Processors (digital logic), memory, RF circuits
  - tight dimensions, integrated materials stacks in small quantities, complex fabrication processes
  - no gold, no Silver, no REE
  - challenge for LCA and for recycling



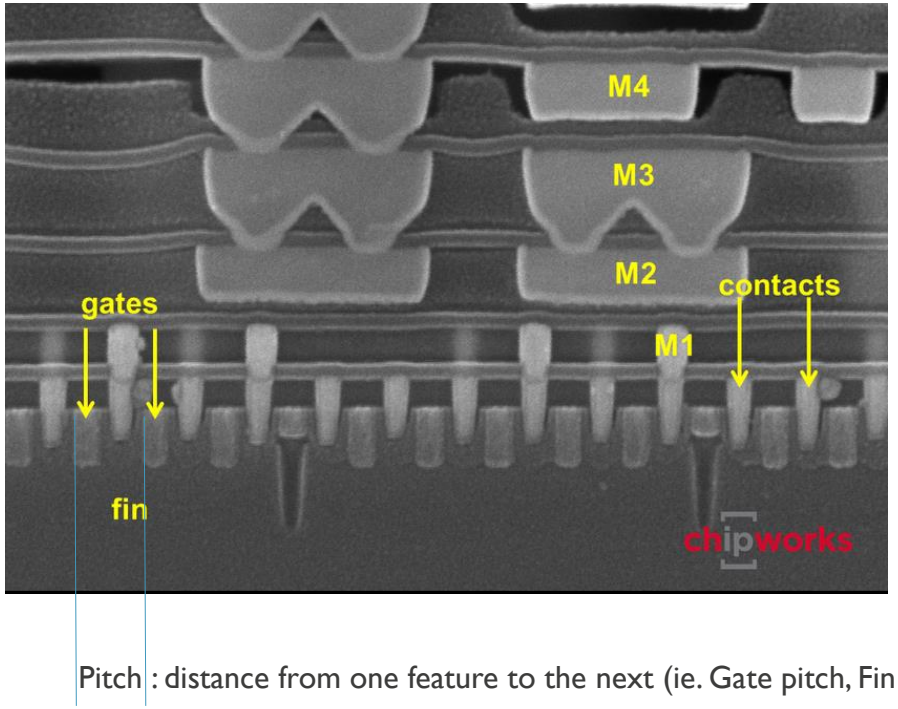


SEMICONDUCTOR MANUFACTURING

PROCESS FLOWS / PROCESS STEPS



- Deposition
- Lithography
- Etching
- Planarization
- ....repeat...
- up to 1500 steps



Pitch : distance from one feature to the next (ie. Gate pitch, Fin pitch, Metal pitch)

IMEC LEUVEN


WORLD-CLASS INFRASTRUCTURE
>12,000 M² CLEANROOM
CAPACITY
CLOSE TO
4,000 SKILLED RESEARCHERS
FROM OVER 90 NATIONALITIES
A
TRUSTED PARTNER FOR
COMPANIES, STARTUPS & ACADEMIA
300 mm pilot line
Nano bio labs
200 mm pilot line
Organic solar cell line
Silicon solar cell line

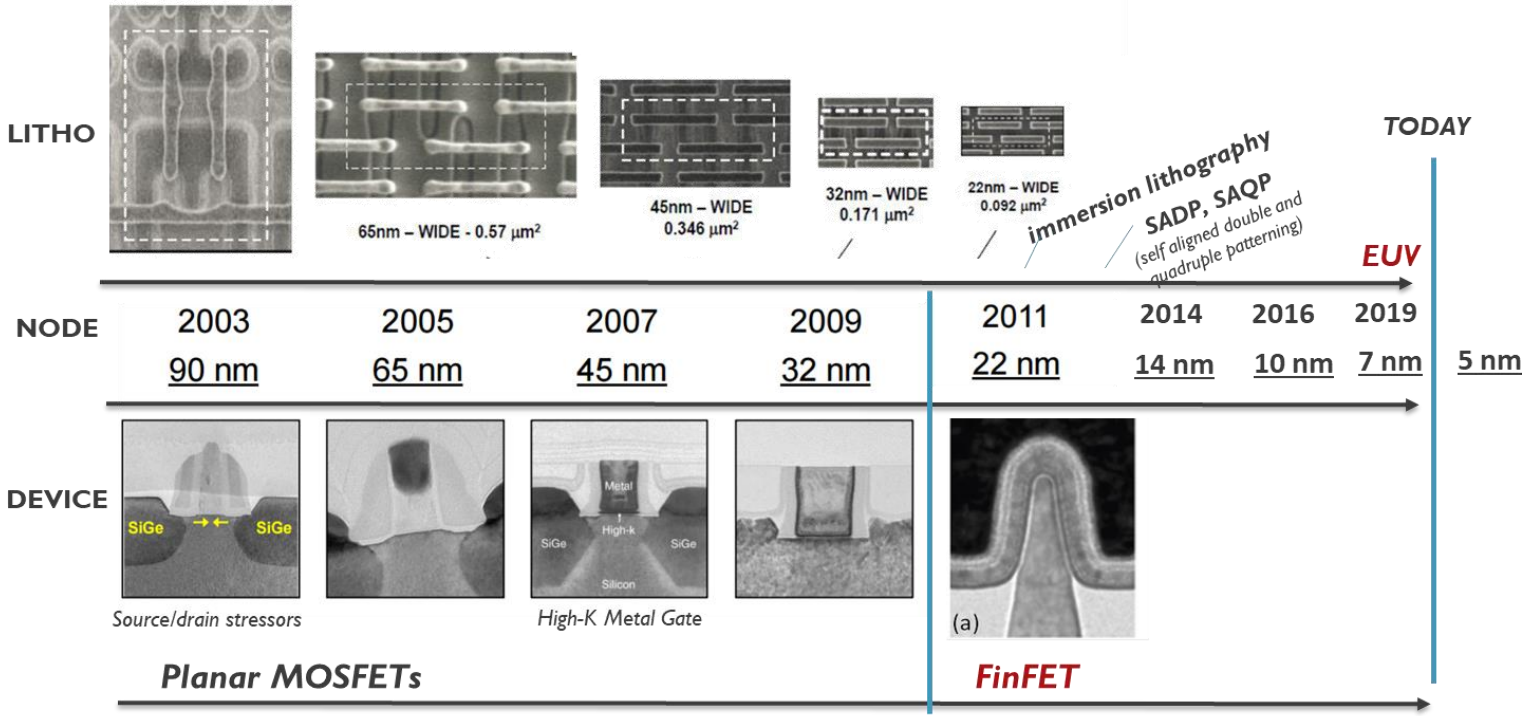
DIGITAL ROADMAP METRICS / SCALING DRIVERS : PPAC

CMOS technology nodes scaling

- **P**OWER : active, dynamic power during operation + leakage power : target -40%
- **P**ERFORMANCE : speed, frequency of operation on critical path: target +20%
- **A**REA : logic standard cells area: target -50% (=2x transistors count)
- **C**OST: lower cost in $ per wafer due to area scaling (performance/chip increases)

NUMEROUS INNOVATIONS TO CONTINUE SCALING/MINIATURIZATION

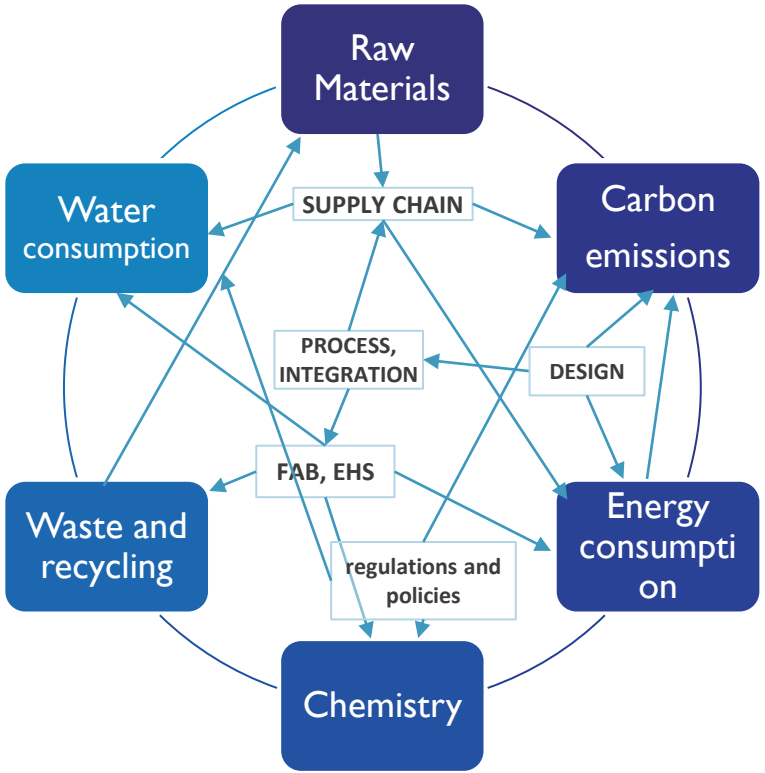
LITHOGRAPHY, PROCESS, DEVICE, MATERIALS, ...



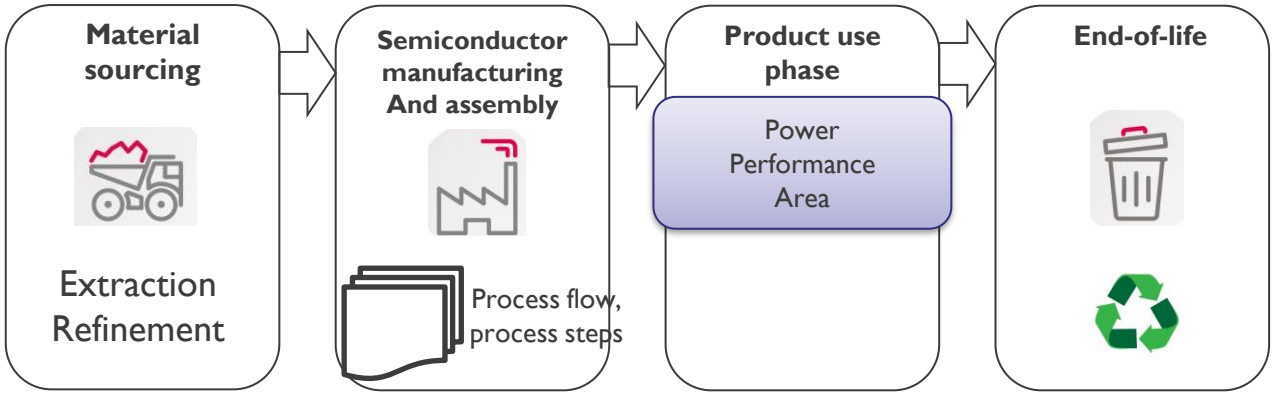
- PPAC metrics are the driving forces for the logic technology innovation since 50 years
- For a long time, dimensional scaling came “naturally”, but since some nodes the manufacturing/ processing effort has increased to support these targets
- We are reaching a turning point with new types of scaling (3D, neuromorphic computing, magnetic RAMs, ferroelectrics...)
- The complexity lead to holistic approaches : Design Technology Co-optimization methodologies and tools

ENVIRONMENTAL COST

- Monitored separately in/after production in fabs
- Standards and targets
- Environment, Health and Safety = EHS
- Multi dimensional / transversal topic to bring it to design phase

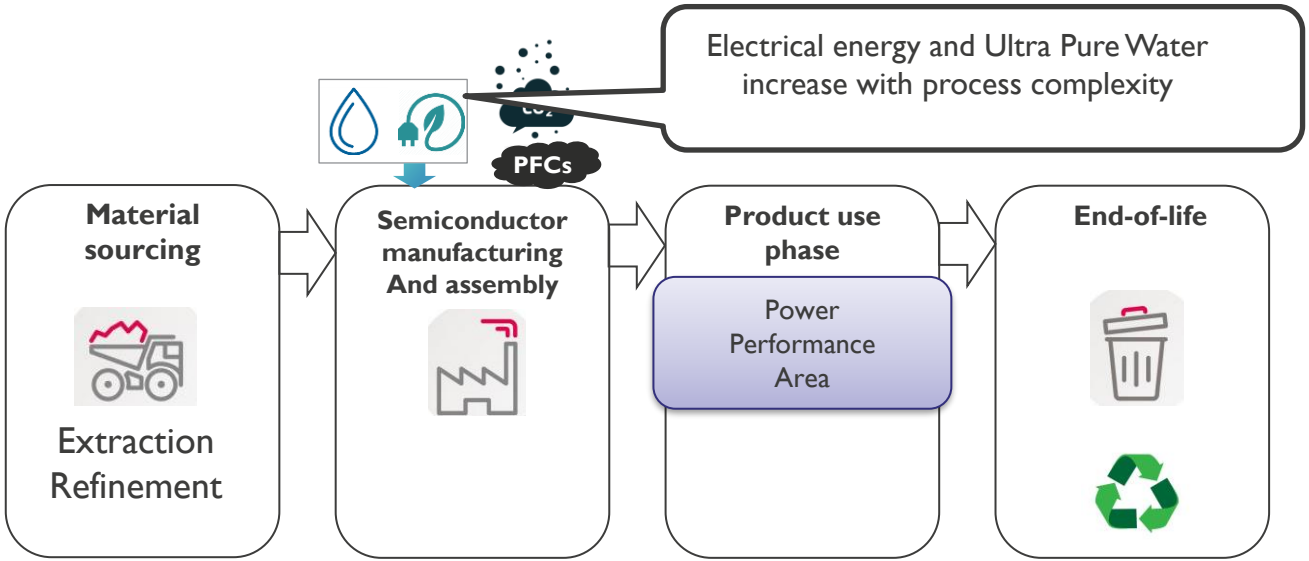


METRICS ACROSS THE SEMICONDUCTORS VALUE CHAIN



METRICS ACROSS THE SEMICONDUCTORS VALUE CHAIN

FOOTPRINT OF FAB ELECTRICITY, WATER AND GAS EMISSIONS



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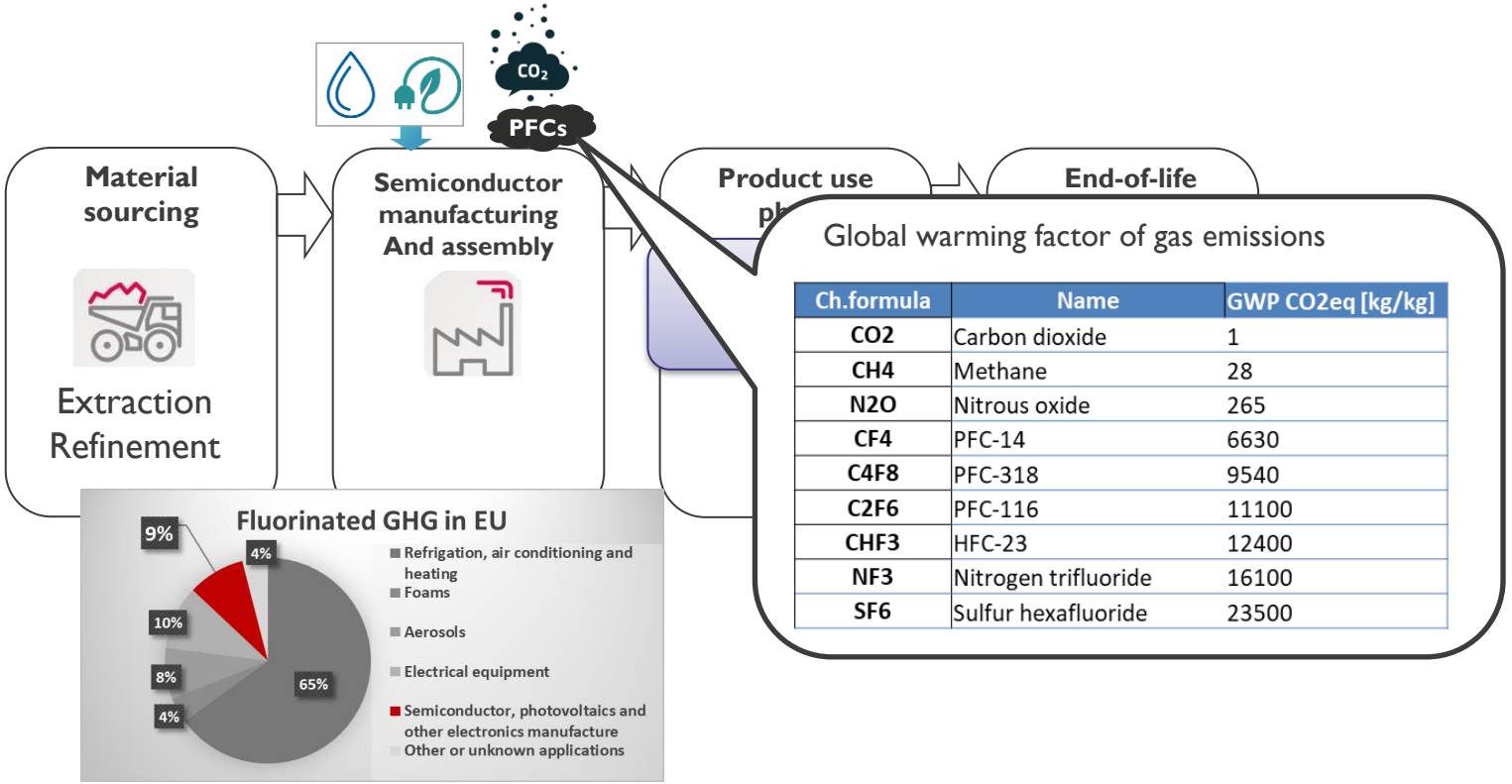
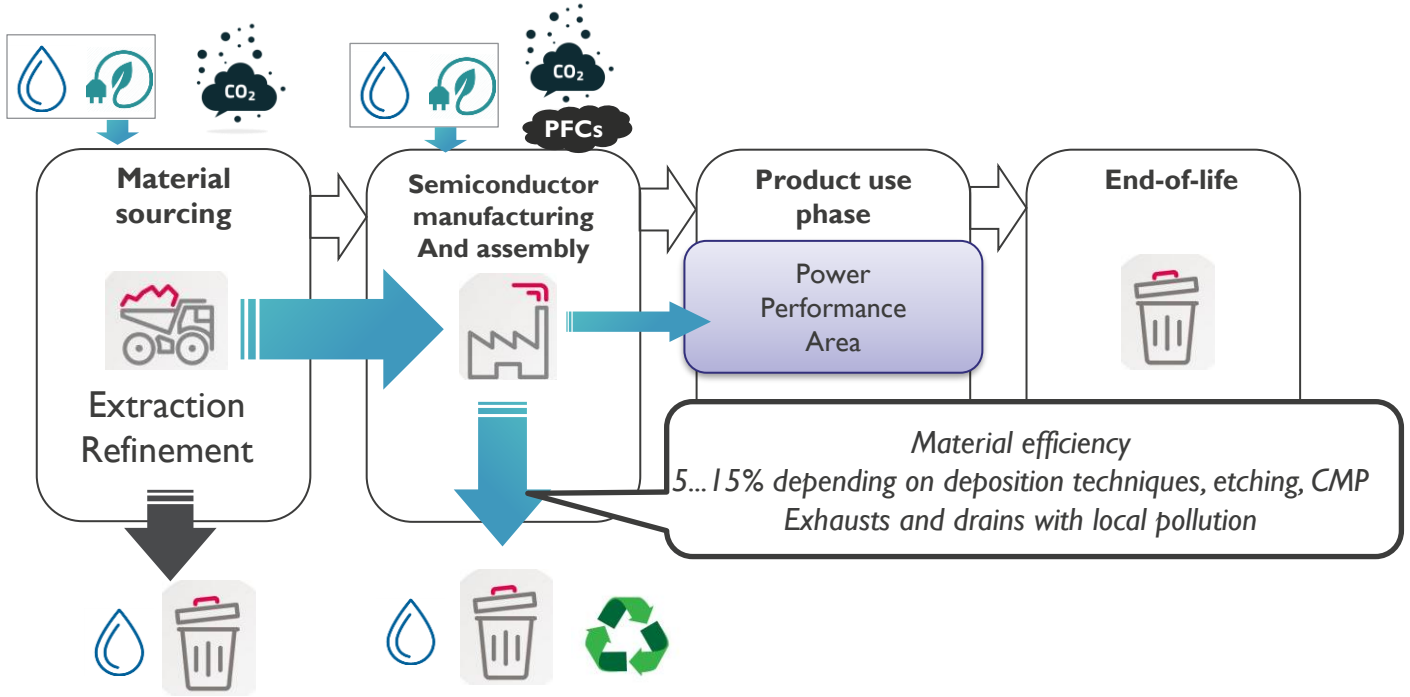


Global warming factor of gas emissions

Ch.formula	Name	GWP CO2eq [kg/kg]
CO2	Carbon dioxide	1
CH4	Methane	28
N2O	Nitrous oxide	265
CF4	PFC-14	6630
C4F8	PFC-318	9540
C2F6	PFC-116	11100
CHF3	HFC-23	12400
NF3	Nitrogen trifluoride	16100
SF6	Sulfur hexafluoride	23500

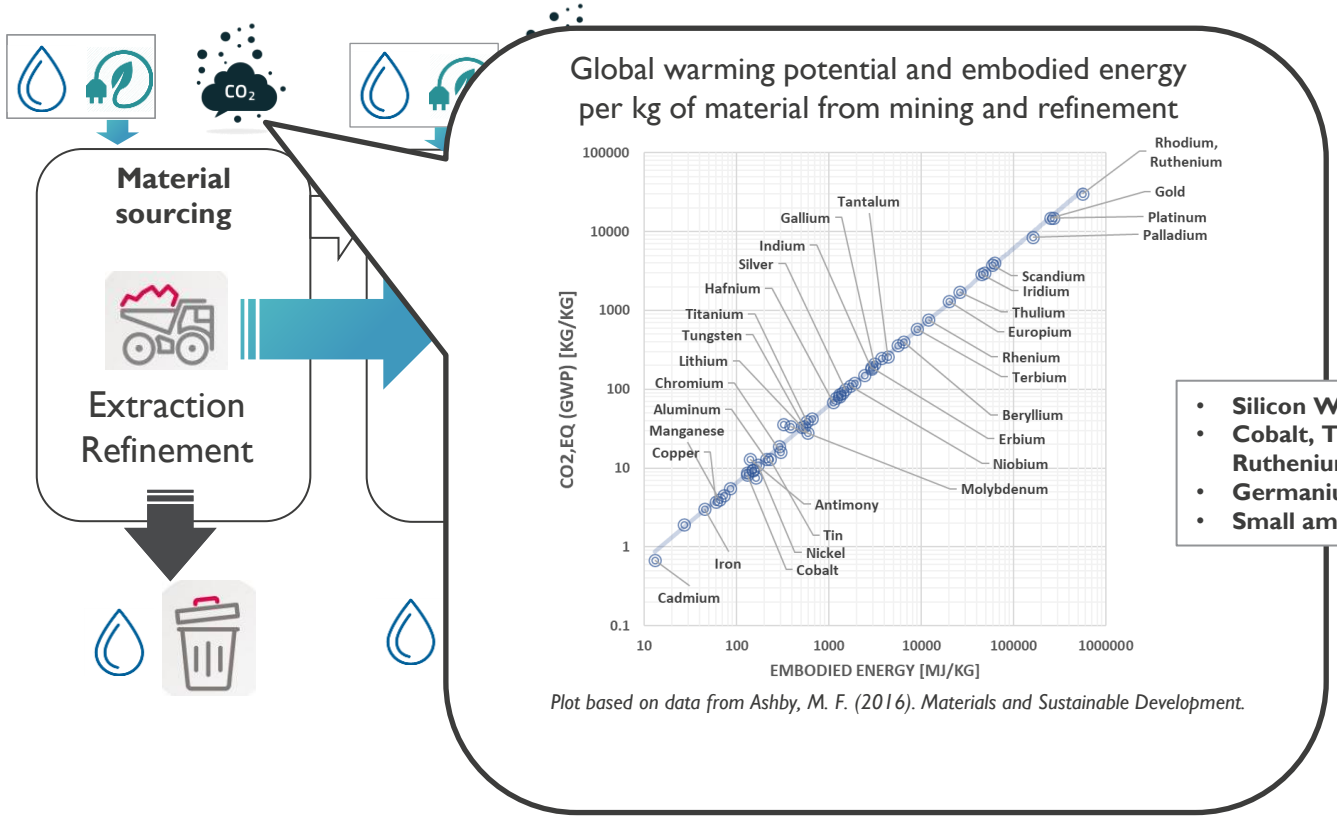
METRICS ACROSS THE SEMICONDUCTORS VALUE CHAIN

FOOTPRINT OF MATERIAL SOURCING AND IMPORTANCE OF MATERIAL EFFICIENCY IN THE FAB



METRICS ACROSS THE SEMICONDUCTORS VALUE CHAIN

FOOTPRINT OF MATERIAL SOURCING

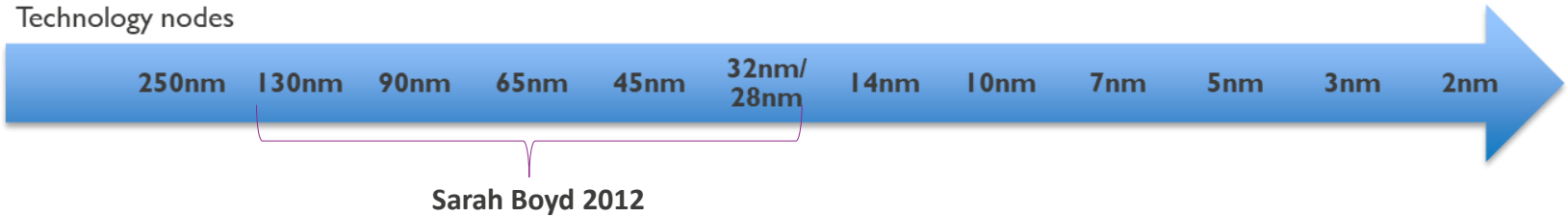


Plot based on data from Ashby, M. F. (2016). Materials and Sustainable Development.

- **Silicon Wafer footprint**
- **Cobalt, Tungsten, Ruthenium ...**
- **Germanium channels**
- **Small amounts**

LCA OF SEMICONDUCTORS

DIFFICULTY OF DATA COLLECTION



- Few analysis available
- Complexity of the fabrication, multiple technologies
- Complexity of the supply chain
- Legal challenge related to IPs: Most players have access to part of the information

MOTIVATIONS FOR ENVIRONMENTAL ASSESSMENTS
FROM INDUSTRY

- Local and global policies (RoHS, Carbon tax, GHG emissions trading, Product efficiency regulations)
- Cost, Supply chain sustainability, Business continuity
- Public image, concerns on climate change and/or local pollution

Existing efforts

- Environment, Health and Safety
- Sustainability teams inside companies, Corporate Social Responsability reports
- Coalitions, Grouped initiatives : World Semiconductor Council (WSC), Responsible Business Alliance (RBA)
- Collaborations with companies or universities for LCA (TSMC, Sony, Intel)

SUSTAINABILITY FOR SEMICONDUCTOR TECHNOLOGIES

- Semiconductor industry has a long running expertise in EHS but disconnected from the design phase
- Sustainability should become a roadmap metric, to identify early bottlenecks and guide choices co-optimized with functionality
- A bottom up approach based on process flows and process steps is needed
- Data collection for semiconductor manufacturing is a challenge
- Needs for transversal collaborations, construction of an ecosystem : industry (including suppliers, foundries and fabless), academy, regulations